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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,585	11/26/2003	Victor C. Dardzinski	81771	7600

35617 7590 12/01/2005

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EXAMINER	
NGUYEN, SANG H	
ART UNIT	**PAPER NUMBER**
2877	

DATE MAILED: 12/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,585	DARDZINSKI, VICTOR C.	
	Examiner	Art Unit	
	Sang Nguyen	2877	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14 and 15* is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☒ Claim(s) *3-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/05/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I (claims 1-15) in the reply filed on 10/19/05 is acknowledged.

Response to Amendment

Applicant's amendment filed on 10/19/05 has been entered. It is noted that that application contains claims 1-15 and claim 16 has been canceled by the amendment on 10/19/05.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 01/05/05. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Oath/Declaration

The oath/declaration filed on 04/29/04 is acceptable.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiyama et al (U.S. Patent No. 6,797,975) in view of Solarz (U.S. Patent No. 6,661,580).

Regarding claim 1; Nishiyama et al teaches an apparatus for inspecting a semiconductor wafer, said apparatus comprising:

(a) a first light source (101 of figure 1 as indicate an illumination optical system) for producing a first beam of light (figure 1), said first beam of light illuminating an area (figure 1) on the semiconductor wafer (102 of figure 1),

(b) a main imaging camera (104 of figure 1, as indicate a light detector unit) disposed above the semiconductor wafer (102 of figure 1) for detecting light scattered (col.5 lines 25-27) from the area illuminated by the first beam of light of the first light source (101 of figure 1), and

(c) a main imaging lens (103 of figure 1, as indicate a detection optical system [see col.6 lines 1-9 and 25-35 and col.24 lines 53-57]) for imaging the area on the semiconductor wafer (102 of figure 1) illuminated by the first beam of light onto said main imaging camera (104 of figure 1), and

(d) an auto-focus system (having an auto-focus illumination [108 of figure] and an auto-focus light receiver [109 of figure 1]) to compensate for vertical deviations (col.5 lines 32-41) in the topology of said semiconductor wafer (102 of figure 1), said auto-focus system ensuring that said main imaging lens (103 of figure 1) images the area on said semiconductor wafer onto said main imaging lens in focus (col.5 lines 32-41), said auto-focus system comprising,

(i) a second light source considered to be auto-focus illumination (108 of figure) for producing a second beam of light (figure 1), said second beam of light reflecting off the area on the semiconductor wafer (102 of figure 1), and

(ii) a sensor considered to be auto-focus light receiver (109 of figure 1) for detecting light reflected from the semiconductor wafer (figure 1) by the second beam of light of the second light source (108 of figure 1). See figures 1-35.

U.S. Patent Sep. 28, 2004 Sheet 1 of 21 US 6,797,975 B2

FIG. 1

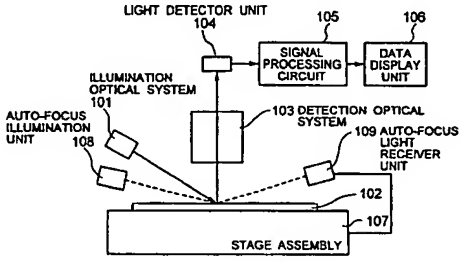
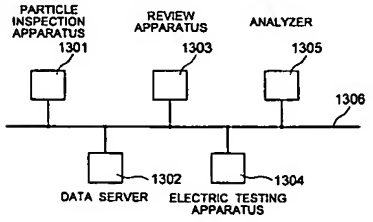


FIG. 2



Nishiyama et al discloses all of features of claimed invention except for a second light source with associated optics and a sensor with associated optics in the auto-focus system. However, Solarz teaches that it is known in the art to provide an optical inspection system for inspecting a semiconductor wafer specimen (106 of figure 1) comprising an auto-focus device (114 of figure 1) having a second light source (116 of figure 1) with associated optics considered to be objective lens (104 of figure 1) and

image grating (128a of figure 1), and a sensor (120 of figure 1) with associated optics considered to be objective lens (104 of figure 1) and image grating (126a of figure 1).

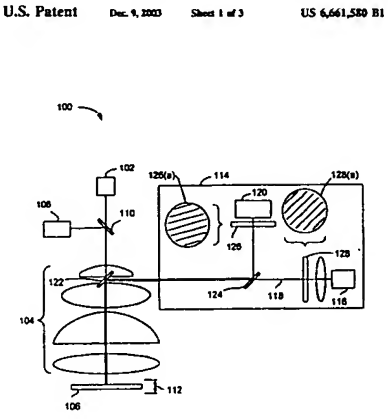


FIG. 1

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine Nishiyama et al's apparatus and method with a second light source with associated optics and a sensor with associated optics in the auto-focus system as taught by Solarz for the purpose of producing accurate inspection results, specimen should be positioned within a very depth of field (col.1 lines 50-53) and operating range of the inspection system and slightly raising the lower end of the operational range (col.2 lines 29-30), and wavelength of the auto-focusing light beam is proximate to or within the operational bandwidth (col.2 lines 40-41).

Regarding claim 2; Nishiyama et al teaches the sensor is a linear position sensor considered to be CCD linear sensor or a position sensor (col.6 lines18-24 and 58-59).

Allowable Subject Matter

Claims 3-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art made of record, taken alone or in combination, and considered pertinent to the applicant's disclosure does not teach or fails discloses or render obvious an apparatus for inspecting a semiconductor wafer comprising all the specific elements with the specific combination including of said auto-focus system further comprises a circuitry for converting the light detected by said linear position sensor into a voltage which is proportional to the relative vertical position of the area of the semiconductor wafer in set forth claim 3.

Claims 14- 15 are allowed.

The following is an examiner's statement of reasons for allowance:

As to independent claim 14 are allowable over the prior art for at least the reason that the prior art of record, taken alone or in combination, fails discloses or render obvious a method for inspecting an area of a semiconductor wafer using a wafer inspecting apparatus comprising all the specific elements with the specific combination including of said method comprising the steps of: (a) examining the vertical position of the illuminated area of said semiconductor wafer using said auto-focus system (figures

1-3), said auto-focus system yielding an output voltage in response thereto, and (b) displacing the relative vertical position of the illuminated area of said semiconductor wafer using said output voltage in combination with the rest of the limitation of claim 14.

As to independent claim 15 are allowable over the prior art for at least the reason that the prior art of record, taken alone or in combination, fails discloses or render obvious a method for inspecting an area of a first semiconductor wafer using a wafer inspecting apparatus comprising all the specific elements with the specific combination including of said method comprising the steps of: (a) providing a second semiconductor wafer, (b) examining the second wafer using said auto-focus system so as to yield a surface contour map for said second wafer, and (c) examining the first semiconductor wafer using said wafer inspection apparatus, wherein the position of the first patterned semiconductor wafer is displaced relative to said imaging lens based upon the surface contour map for said second wafer in combination with the rest of the limitation of claim 15.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kato (JP 2003262782) discloses position detector and auto-focus apparatus and recorder; Stanke et al (6563586) discloses wafer metrology apparatus

and method; Dotan (6407373) discloses apparatus and method for reviewing defects on an object; Tomita et al (6384909) discloses defect inspection method and apparatus for silicon wafer; or Finarov (5604344) discloses autofocusing microscope having a pattern imaging system

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sang Nguyen whose telephone number is (571) 272-2425. The examiner can normally be reached on 9:30 am to 7:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory J. Toatley, Jr. can be reached on (571) 272-2800 ext. 77. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SN

November 20, 2005

Sanguyen

Patent Examiner
Sang Nguyen
Art Unit 2877